

### REMARKS

Examiner Pompey is to be thanked for careful review of the pending application.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 1, 3-6, and 8-10 remain in this application. Claims 1 and 6 are amended herein. No claims have been allowed. Claims 2 and 7 have been withdrawn

### *Claim Rejections - 35 U.S.C. § 112*

2. The Examiner has rejected Claims 1-10 under 35 U.S.C. § 112 because the specification, while being enabling for a "first high temperature oxidation step...to prevent out-diffusion of nitrogen species ...", does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with applicant's claims.

In response, applicant has amended applicant's claims 1 and 6 to claim applicant's invention as described in applicant's specification, clarifying applicant's invention of employing a first high temperature oxidation step to prevent out-diffusion of nitrogen species.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of Claims 1-10 under 35 U.S.C. § 112 as failing to enable a person

skilled in the art pertinent to the invention to make the invention commensurate in scope with the claims, be withdrawn..

3. The Examiner has applied previous rejection of Claims 1, 3-6 and 8-10 to applicant's invention under 35 U.S.C. §103(a) as being unpatentable over Higashitani et al. (U.S Patent No. 5,637,528; hereinafter "Higashitani".) in view of Wolf (Silicon Processing in the VLSI Era , Vol. 1, pg.209-10, hereinafter "Wolf"), and under 35 U.S.C §102as being anticipated by Liu et al. (U.S. Patent No. 5,739,063, hereinafter "Liu").

Applicant acknowledges in general the teachings of Higashitani et al. in view of Wolf, and of Liu, .as cited by the Examiner

In response, applicant respectfully submits that the teachings of Higashitani et al. in view of Wolf do not disclose singly or in combination the formation, by oxidation at high temperatures, of silicon oxide layers with minimal inclusion therein of impurity phases with deleterious properties as claimed in applicant's thrice amended claim 1 and four times amended claim 6. Therefore, the citation of Higashitani et al. in view of Wolf over applicant's claims is not properly anticipatory, and may not be properly combined as a basis for rejection of applicant's thrice amended claim 1 and four times amended claim 6. Similarly, the citation of Higashitani et al. in view of Wolf may not properly be combined as a basis for rejection of applicant's claim 3-5 and 8-10. Applicant's Claims 3-5 and 8-10 are dependent on applicant's thrice amended base claim 1 and four times amended base claim 6 respectively, and contain each and every limitation thereof.

Further in response, applicant respectfully submits that the key limitation of applicant's invention, which is the formation of a silicon oxide layer on a silicon substrate in an oxidizing environment at least above a minimum temperature, below which temperature are formed deleterious impurity phases within the silicon oxide dielectric layers, is not taught by Liu . Therefore, since each and every limitation within applicant's invention as disclosed and claimed within applicant's amended claims 1 and 6 is neither claimed nor disclosed by Liu et al., applicant asserts that applicant's thrice amended claim 1, four times amended claim 6, and dependent claims 3-5 and 8-10 may not be properly be rejected under 35 U. S. §102 as being anticipated by Liu ..

In light of the foregoing responses, applicant respectfully requests that the Examiners rejection of applicant's thrice amended claim 1, claims 3-5, four times amended claim 6 and claims 8-10 under 35 U. S. §103 as being unpatentable over Higashitani et al. in view of Wolf et al. be withdrawn. Likewise, applicant respectfully requests that the Examiner's rejection under 35 U.S.C. §102 of applicant's thrice amended claim 1, four times amended claim 6, and dependent claims 3-5 and claims 8-10 as being anticipated by Liu be withdrawn.

### ***Discussion***

With respect to the Examiner's citation of the teaching of Liu et al., Higashitani et al. and Wolf , applicant respectfully submits that there is not specifically discussed, disclosed or claimed in any of the aforementioned references employment of an oxidizing method such that formation and annealing of a silicon oxide layer are

accomplished with beneficial effects such as control of the rate of oxidation and formation of silicon oxide with desired properties simultaneous with minimization of deleterious formation of impurity species related to out-diffusion of nitrogen species from adjacent silicon nitride layers. The significant limitation of thermally oxidizing to minimize nitrogen out-diffusion, as specified in applicant's amended claims 1 and 6, is therefore not taught by any of the cited references singly or in combination, and therefore may not be properly cited in rejection of applicant's claims to applicant's invention.

#### ***Other Considerations***

No fee is due as a result of this amendment.

#### **SUMMARY**

Applicant's invention, as claimed within thrice amended claim 1, claims 3-5, four times amended claim 6 and claims 8-10, is directed toward a method for forming within a silicon semiconductor substrate employed within a microelectronics fabrication a silicon oxide dielectric layer employed as a field oxide (FOX) isolation layer by local dry thermal oxidation of the silicon substrate. In conjunction with applicant's claims 1 and 6 as amended, the prior art of record employed in rejection of applicant's claims to applicant's invention neither claims singly nor in combination each and every limitation within applicants thrice amended claim 1 and four times amended claim 6, or in the original claims 3-5 and 8-10.

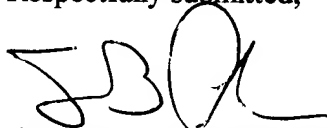
TSMC 98-262  
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### **CONCLUSION**

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, is respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 845-452-5863 or Mr. George Saile, Esq. (Reg. No. 19,572) at 845-452-5863, at the Examiner's convenience.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'SBA', written over a horizontal line.

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**In the Claims**

Claims 1 and 6 are amended as follows:

1.(THRICE AMENDED) A method for forming within a silicon semiconductor substrate employed within a microelectronics fabrication a silicon oxide dielectric layer comprising:

providing a silicon semiconductor substrate;

forming over the silicon semiconductor substrate a patterned silicon nitride mask layer; and

oxidizing the silicon semiconductor substrate locally at a first oxidation temperature of at least above 1100 degrees centigrade through the silicon nitride mask pattern, to form silicon oxide dielectric layers which [to] prevent out-diffusion of nitrogen species from the silicon nitride mask layer, thereby minimizing [, and minimize] formation of silicon oxynitride inclusions within the silicon oxide layers. [; and]

[oxidizing the silicon substrate further at a second temperature no greater than 1100 degrees centigrade, as desired to form greater thickness of said silicon oxide dielectric layers.]

6. ( FOUR TIMES AMENDED) A method for forming within a silicon semiconductor substrate employed within an integrated circuit microelectronics fabrication a silicon oxide dielectric field oxide (FOX) isolation layer comprising:

providing a silicon semiconductor substrate;

forming upon the silicon semiconductor substrate a silicon oxide pad oxide layer;

forming upon the silicon oxide pad oxide layer a patterned silicon nitride mask layer;

oxidizing the silicon substrate locally at a first temperature of at least above 1100 degrees centigrade, through the patterned silicon nitride mask layer to form silicon oxide dielectric field oxide (FOX) isolation layers which [to] prevent out-diffusion of nitrogen species from the silicon nitride mask layer, thereby minimizing [and minimize] formation of silicon oxynitride inclusions within the silicon oxide [dielectric] layers; and

oxidizing the silicon substrate further at a second temperature no greater than 1100 degrees centigrade, as desired to form greater thickness of [said] silicon oxide [dielectric] layers.